

AMENDMENTS TO THE CLAIMS

Claims 1- 55 (canceled).

56. (Currently Amended) A method of ~~recording an identity of~~ operating a memory device comprising:

applying a programming voltage between a respective drain and gate of a transistor disposed within said memory device, and said transistor having a gate threshold adapted to transition from a first value to a second value in response to said programming voltage, whereby said first value corresponds to a first identity and said second value corresponds to a second identity; and

applying a read voltage to a gate of said transistor, wherein said read voltage is between said first value and said second value.

57. (Currently Amended) A method of reading an identity of a memory device comprising:

applying a read voltage to a gate of a transistor having a programmed gate threshold voltage for a time interval, said transistor disposed within said memory device wherein said applied read voltage is between two possible threshold voltage values for said transistor;

reading a conductivity state of said transistor during said time interval; and

perceiving an identity of said memory device according to said conductivity state.

58. (Previously Presented) A method of remapping a defective memory cell address comprising:

applying a programming voltage between a gate and a source of a programmable transistor and thereby changing a gate threshold of said transistor to correspond to a programmed state;

applying a read signal voltage to said gate of said transistor, causing said transistor to output a signal corresponding to said programmed state;

communicating said output signal of said transistor to an input of an address decoder; and

changing an output of said address decoder in response to said communicated signal so as to select a non-defective memory cell.

59. (Previously Presented) The method of claim 56, wherein said applied programming voltage is approximately 6V.

60. (Previously Presented) The method of claim 56, wherein said applying a programming voltage comprises application of a voltage source for approximately five seconds.

61. (Previously Presented) The method of claim 56, wherein said first value corresponds to a normal threshold voltage for said transistor.

62. (Previously Presented) The method of claim 61, wherein said second value is higher than said first value.

63. (Previously Presented) The method of claim 56, wherein said first value is approximately .7V and said second value is approximately 1.5V.

64. (Currently Amended) The method of claim 56, wherein said first identity corresponds to said gate being in an “on” state and said second identity corresponds to said ~~transistor~~ gate being in an “off” state.

65. (Currently Amended) The method of claim 56, wherein ~~the step of~~ said applying a programming voltage between a respective drain and gate of a transistor comprises applying one pre-determined voltage value to said gate and applying a second pre-determined voltage value to said drain.

66. (Previously Presented) The method of claim 65, wherein said first pre-determined voltage value is applied via a first signal line and said second pre-determined voltage value is applied via a second signal line.

67. (Previously Presented) The method of claim 66, wherein said first pre-determined voltage value is approximately 6V, and said second pre-determined voltage value is approximately 4.5V.

68. (Currently Amended) The method of claim 56 further comprising ~~the steps of:~~
generating a response current at said transistor in response to said applied programming voltage; and

applying said response current to a latching circuit so as to record the identity of said transistor.

69. (Previously Presented) The method of claim 57, further comprising grounding a source of said transistor.

70. (Currently Amended) The method of claim 69, wherein ~~said step of said~~ grounding of said source of said transistor is performed simultaneously with the ~~step~~ act of applying a read voltage to said gate.

71. (Currently Amended) The method of claim 57, wherein ~~the step of said~~ reading a conductivity state of said transistor comprises determining the state of an associated output node of an associated latch circuit.

72. (Currently Amended) The method of claim 57, wherein said ~~applied read voltage is greater than the normal~~ two possible threshold values comprise a normal threshold voltage value of said transistor and an increased threshold voltage value of said transistor that is approximately twice the normal threshold voltage value of said transistor.

73. (Currently Amended) The method of claim 57, wherein said ~~applied read voltage is between~~ two possible threshold voltage values for said transistor are within the range of about 0.7V to about 2.0V.

74. (New) The method of claim 57, wherein said reading a conductivity state of said transistor comprises:

applying a voltage between a source and a drain of said transistor; and

sensing a responsive current through said transistor.

75. (New) The method of claim 74, wherein said sensing a responsive current through said transistor comprises applying the responsive current to an input node of a sensing latch circuit.

76. (New) The method of claim 75, further comprising creating an output by inverting the responsive current at the input node and applying the output to an output node.

77. (New) The method of claim 76, wherein the output at the output node represents either an “on” or an “off” state of said transistor gate.